What is claimed is:

1. A synchronous mirror delay circuit for generating an internal clock signal synchronized with an external clock signal, the synchronous mirror delay circuit comprising:

a clock buffer circuit for generating a reference clock signal in response to the external clock signal;

a delay monitor circuit for delaying the reference clock signal;

a forward delay array for delaying an output clock signal of the delay monitor circuit to generate delay clock signals;

a mirror control circuit for receiving the delay clock signals and the reference clock signal and detecting one delay clock signal synchronized with the reference clock signal among the delay clock signals;

a backward delay array for delaying the detected delay clock signal to output a synchronous clock signal;

a delay circuit for delaying an asynchronous clock signal output through the forward delay array; and

a clock driving circuit for outputting the delayed asynchronous clock signal as the internal clock signal when the reference clock signal is not synchronized with one of the delay clock signals.

2. The synchronous mirror delay circuit of claim 1, wherein the forward delay array comprises serially-connected delay units having the same delay time.

3. The synchronous mirror delay circuit of claim 2, wherein the mirror control circuit comprises phase detectors corresponding to respective delay units, the phase detectors

receiving the reference clock signal and the delay clock signal outputted from the corresponding delay unit.

4. The synchronous mirror delay circuit of claim 3, wherein the delay circuit is inactivated by an output signal of the last phase detector when the last phase detector detects the delay clock signal synchronized with the reference clock signal.

5. The synchronous mirror delay circuit of claim 1, wherein the clock driving circuit outputs a synchronous clock signal output from the backward delay array as the internal clock signal when the reference clock signal is synchronized with one of the delay clock signals.

6. The synchronous mirror delay circuit of claim 1, wherein the delay monitor circuit comprises:

a second clock buffer circuit;

a first driving circuit; and

a first regenerator circuit.

7. The synchronous mirror delay circuit of claim 1, wherein the clock driving circuit comprises:

a second driving circuit; and

a second regenerator circuit.

8. A semiconductor integrated circuit device operating in synchronization with an external clock signal, the semiconductor integrated circuit device comprising:

a synchronous mirror delay circuit for generating an internal clock signal synchronized

with the external clock signal; and

a data input/output circuit for inputting and outputting data in synchronization with the internal clock signal,

wherein the synchronous mirror delay circuit comprises:

a clock buffer circuit for generating a reference clock signal in response to the external clock signal;

a delay monitor circuit for delaying the reference clock signal;

a forward delay array for delaying an output clock signal of the delay monitor circuit to generate delay clock signals;

a mirror control circuit for receiving the delay clock signals and the reference clock signal and detecting one delay clock signal synchronized with the reference clock signal among the delay clock signals;

a backward delay array for delaying the delay clock signal detected by the mirror control circuit and outputting a synchronous clock signal;

a delay circuit for delaying an asynchronous clock signal output through the forward delay array; and

a clock driving circuit for outputting the delayed asynchronous clock signal as the internal clock signal when the reference clock signal is not synchronized with one of the delay clock signals.

9. The semiconductor integrated circuit device of claim 8, wherein the forward delay array comprises serially-connected delay units having the same delay time.

10. The semiconductor integrated circuit device of claim 9, wherein the mirror control circuit comprises phase detectors corresponding to the delay units, the phase detectors

receiving the reference clock signal and the delay clock signal outputted from the corresponding delay unit.

11. The semiconductor integrated circuit device of claim 10, wherein the delay circuit is inactivated by an output signal of the last phase detector when the last phase detector detects the delay clock signal synchronized with the reference clock signal.

12. The semiconductor integrated circuit device of claim 8, wherein the clock driving circuit outputs a synchronous clock signal output from the backward delay array as the internal clock signal when the reference clock signal is synchronized with one of the delay clock signals.

13. A method for generating an internal clock signal synchronized with an external clock signal, the method comprising the steps of:

generating a reference clock signal in response to the external clock signal;

delaying the reference clock signal;

sequentially delaying an output clock signal to generate an asynchronous clock signal and delay clock signals;

detecting one delay clock signal synchronized with the reference clock signal among the delay clock signals;

delaying the detected delay clock signal to output a synchronous clock signal; and

outputting the asynchronous clock signal as the internal clock signal, when the reference clock signal is not synchronized with one of the delay clock signals.

14. The method of claim 13, further comprising outputting the synchronous clock signal as the internal clock signal when the reference clock signal is synchronized with one of the delay clock signals.

15. The method of claim 13, wherein the asynchronous clock signal is not generated when the last delayed delay clock signal of the delay clock signals is synchronized with the reference clock signal.